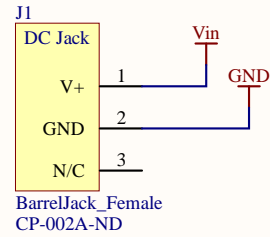
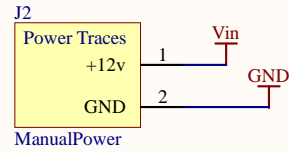


## Power Input

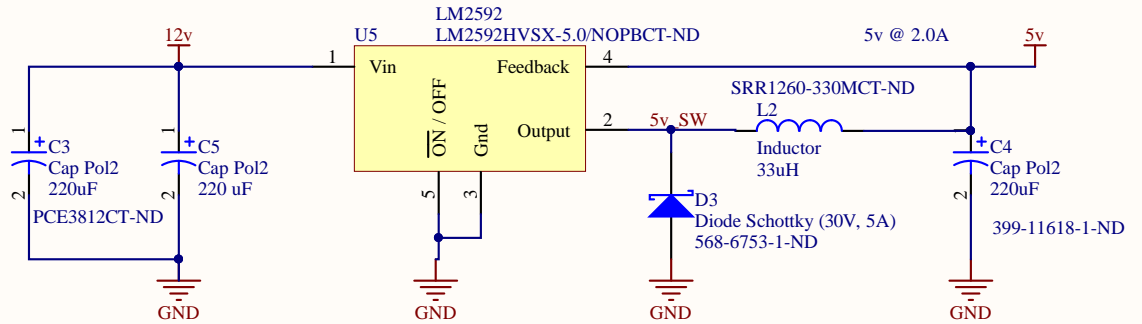
+12v input



Backup for Barrel Jack

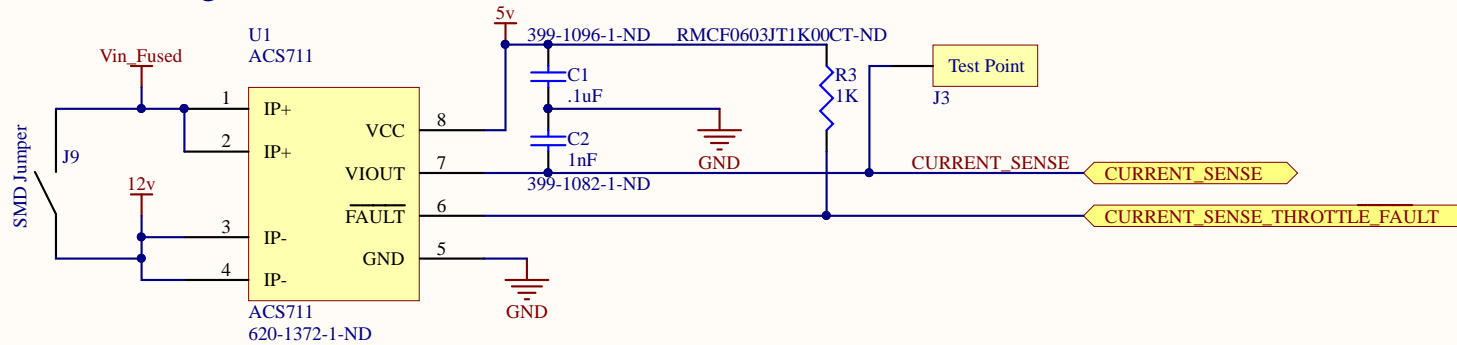


## Voltage Regulation

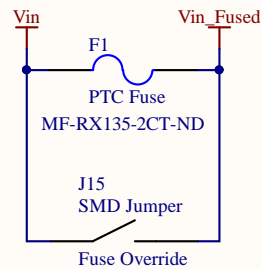


Note: This needs to be a schottky diode

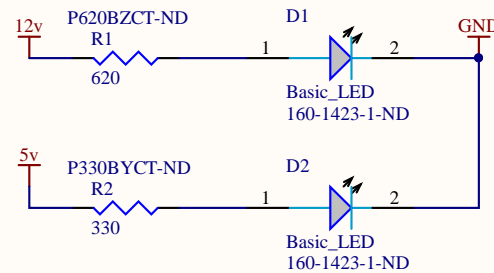
## Current Sensing



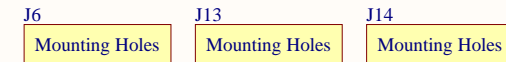
## Fusing



## Power LEDs



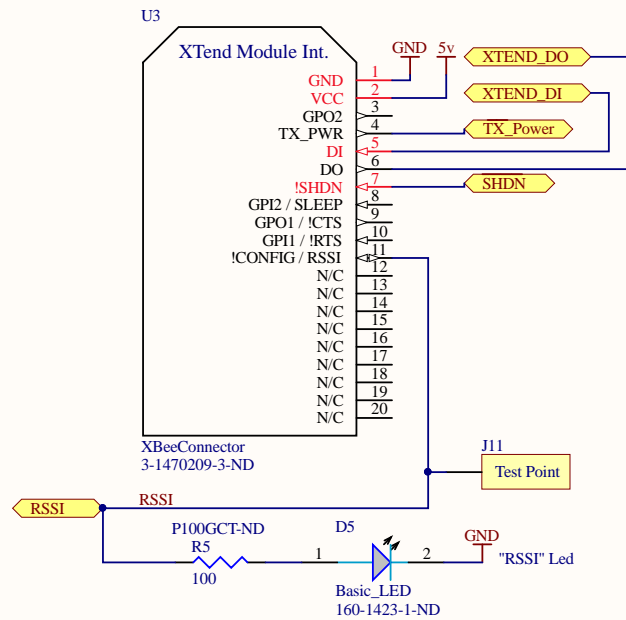
## Miscellaneous Hardware



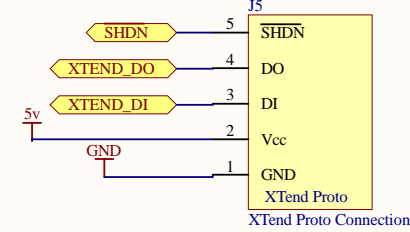
|  |                          |                              |   |
|--|--------------------------|------------------------------|---|
| Title <b>PowerSupplies.SchDoc</b>  |                          |                              | <i>Ocean Mixing Group</i><br><i>Oregon State University</i><br><i>Corvallis, OR</i> |
| Size: <b>A4</b>  | Number: *                | Engineer: <b>Nick McComb</b> |   |
| Date: <b>11/24/2015</b>  | Time: <b>11:24:49 AM</b> | Sheet <b>1</b> of *          |   |
| File: <b>C:\Users\nrpic_000\Google Drive\PCB Designs\XTendDaughterboard\PowerSupplies.SchDoc</b> |                          |                              |   |

|   |           |          |
|---|-----------|----------|
| Title                                   |           |          |
| Size A                                  | Number    | Revision |
| Date: 11/24/2015                        | Sheet of  |          |
| File: C:\Users\...\PowerSupplies.SchDoc | Drawn By: |          |

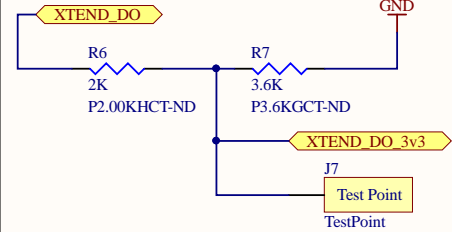
## XTend Connection



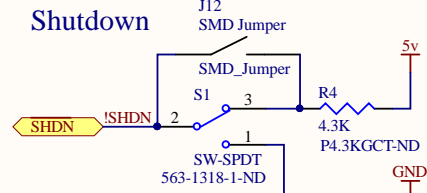
## "Prototyping" Connection



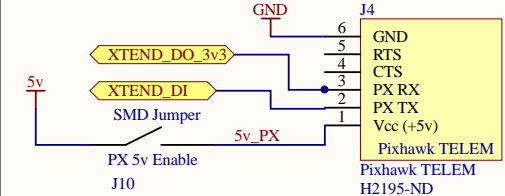
## Logic Level Conversion



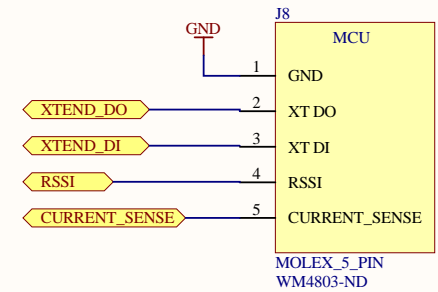
## Shutdown



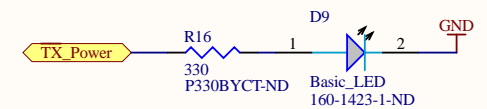
## Pixhawk CONN



## MCU CONN



## TX LED



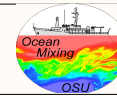
Title RSSIandXTend.SchDoc

Size: A4 Number: \* Engineer: Nick McComb

Date: 11/24/2015 Time: 11:24:49 AM Sheet 2 of \*

File: C:\Users\nrpic\_000\Google Drive\PCB Designs\XTend\Daughterboard\RSSIandXTend.SchDoc

Ocean Mixing Group  
Oregon State University  
Corvallis, OR



Title

Size

A4

Number

Revision

Date: 11/24/2015

File: C:\Users\...\RSSIandXTend.SchDoc

Sheet of

Drawn By:



|                                    |           |        |
|------------------------------------|-----------|--------|
| ENGINEER:                          | TITLE:    |        |
| PCB DESIGNER:                      |           |        |
| DATE:<br>11/24/2015                | PART NO.: | REV:   |
| FILE NAME:<br>Daughterboard.PcbDoc | DWG NO:   | SCALE: |

Boards